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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,253	08/24/2001	James M. Derderian	4830US (01-0106)	2189

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	09/939,253	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 41-67* is/are pending in the application.

4a) Of the above claim(s) *14 -16, 27-30, 34 -36, 41 and 45-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 17-26, 31- 33, 37-39 and 42-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 09/939253 Attorney's Docket #: 4830US(01-0106)
Filing Date: 8/24/01;

Applicant: Derderian

Examiner: Alexander Williams

Applicant's Amendment filed 11/1/07 has been acknowledged. The claims being examined are claims 1 to 13, 17-26, 31 to 33, 37 to 39 and 42 to 44.

This application contains claims 14 to 16, 27 to 30, 34 to 36, 41 and 45 to 67 drawn to an invention non-elected without traverse in Paper No. 11.

Claims 40 and 68 to 102 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 10, 17 and 19 are rejected under 35 U.S.C. 102(e) as anticipated by Nakanishi et al. (U.S. Patent Application Publication # 2001/0013643).

For example, in claim 1, Nakanishi et al. (figures 1 to 12) specifically figure 9 show a semiconductor device for use in a stacked multi-chip assembly, comprising: a semiconductor die **2**; and a dielectric spacer layer **24,25** secured to at least a portion of a surface of said semiconductor die and protruding from the surface substantially a predetermined distance from an adjacent semiconductor die **1** to accommodate a height of at least one laterally extending intermediate conductive element **(solder balls 1a)** located between the semiconductor die, the spacer layer including voids **(space between the two ends of 24,25)** communicating with a lateral periphery thereof.

2. The semiconductor device of claim 1, **Nakanishi et al. show** wherein said spacer layer comprises a plurality of laterally discrete spacers.

3. The semiconductor device of claim 1, **Nakanishi et al.** further comprising: at least one discrete conductive element protruding above a surface of said semiconductor die.

4. The semiconductor device of claim 3, **Nakanishi et al. show** wherein said at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. The semiconductor device of claim 1, **Nakanishi et al. show** wherein said predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

6. The semiconductor device of claim 1, **Nakanishi et al. show** wherein said predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface

of at least one of said semiconductor die and said adjacent semiconductor die.

7. The semiconductor device of claim 1, **Nakanishi et al. show** wherein said spacer layer covers only a portion of said surface.

8. The semiconductor device of claim 7, **Nakanishi et al. show** wherein said spacer layer comprises a pattern.

9. The semiconductor device of claim 7, **Nakanishi et al. show** wherein said spacer layer comprises randomly arranged features.

10. The semiconductor device of claim 1, **Nakanishi et al. show** wherein said spacer layer comprises a material that will adhere to a surface of said adjacent semiconductor die.

17. The semiconductor device of claim 1, **Nakanishi et al.** further comprising: adhesive material on an exposed surface of said spacer layer.

Claims 19, 22 to 26, 33 and 35 to 40 are rejected under 35 U.S.C. 102(e) as anticipated by Foster (U.S. Patent # 6,437,449 B1).

For example, in claim 19, Foster (figures 1 to 4) specifically figure 3 show a semiconductor device assembly, comprising: a first semiconductor device **108**; a nonconfluent spacer layer **216** comprising dielectric material secured to a surface of said first semiconductor device, a second semiconductor device **140** positioned over said first semiconductor device, a surface of said second semiconductor device being secured to said nonconfluent spacer layer; and the second semiconductor device, including a back side secured to the nonconfluent spacer layer.

(13) A spacer of a uniform thickness is provided. The spacer may be of an electrically conductive or a dielectric material, and has a front surface, an opposite back surface, and an outer periphery that is smaller than an inner periphery of the wire bonding pads on the first die. The spacer is mounted on the front surface of the first die such that the spacer is located inside the inner periphery of the wire bonding pads thereon and is electrically isolated therefrom.

22. The semiconductor device assembly of claim 19, Foster **show** wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. The semiconductor device assembly of claim 19, Foster **show** wherein said nonconfluent spacer layer has a substantially uniform thickness.

24. The semiconductor device assembly of claim 19, **Foster** further comprising: at least one discrete conductive element protruding above a surface of at least one of said first and second semiconductor devices and located at least partially between said first and second semiconductor devices.

25. The semiconductor device assembly of claim 24, **Foster show** wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that exceeds a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

26. The semiconductor device assembly of claim 24, **Foster show** wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from

one another a distance that is about the same as or less than a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

33. The semiconductor device assembly of claim 19, Foster **show** wherein said nonconfluent spacer layer comprises a pattern.

35. The semiconductor device assembly of claim 19, Foster further comprising: an adhesive material **216,221** securing said nonconfluent spacer layer to at least one of said surface of said first semiconductor device and said surface of said second semiconductor device.

36. The semiconductor device assembly of claim 35, Foster **show** wherein said adhesive material is located within voids in said nonconfluent spacer layer.

In claim 37, Foster how a substrate 204 upon which one of said first semiconductor device 108 and said second semiconductor device 140 is positioned.

In claim 38, **Foster show** at least one bond pad of at least one of said first semiconductor device **108** and said second semiconductor device **140** is in communication with a corresponding contact area of said substrate **204**.

In claim 39, **Foster show** the substrate comprising at least one of a circuit board, an interposer, another semiconductor device, and leads **204**.

40. The semiconductor device assembly of claim 19, Foster show wherein said nonconfluent spacer layer is positioned between an

active surface of said first semiconductor device and a back side of said second semiconductor device.

Claims 1 to 10, 17, 19 to 26, 33 and 37 to 39 are rejected under 35 U.S.C. 102(b) as anticipated by Vindasius et al. (U.S. Patent # 6,098,278).

For example, in claim 1, Vindasius et al. (figures 1 to 12) specifically figure 15 show a semiconductor device for use in a stacked multi-chip assembly, comprising: a semiconductor die **152**; and a dielectric spacer layer **162** secured to at least a portion of a surface of said semiconductor die and protruding from the surface substantially a predetermined distance from an adjacent semiconductor die **150** to accommodate a height of at least one laterally extending intermediate conductive element **156** located between the semiconductor die, the spacer layer including voids **(space between the two 162's)** communicating with a lateral periphery thereof.

2. The semiconductor device of claim 1, **Vindasius et al. show** wherein said spacer layer comprises a plurality of laterally discrete spacers.

3. The semiconductor device of claim 1, **Vindasius et al.** further comprising: at least one discrete conductive element protruding above a surface of said semiconductor die.

4. The semiconductor device of claim 3, **Vindasius et al. show** wherein said at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. The semiconductor device of claim 1, **Vindasius et al. show** wherein said predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at

least one of said semiconductor die and said adjacent semiconductor die.

6. The semiconductor device of claim 1, **Vindasius et al. show** wherein said predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

7. The semiconductor device of claim 1, **Vindasius et al. show** wherein said spacer layer covers only a portion of said surface.

8. The semiconductor device of claim 7, **Vindasius et al. show** wherein said spacer layer comprises a pattern.

9. The semiconductor device of claim 7, **Vindasius et al. show** wherein said spacer layer comprises randomly arranged features.

10. The semiconductor device of claim 1, **Vindasius et al. show** wherein said spacer layer comprises a material that will adhere to a surface of said adjacent semiconductor die.

17. The semiconductor device of claim 1, **Vindasius et al.** further comprising: adhesive material on an exposed surface of said spacer layer.

For example, in claim 19, Vindasius et al. (figures 1 to 18) specifically figure 15 show a semiconductor device assembly, comprising: a first semiconductor device **152**; a nonconfluent spacer layer **162** comprising dielectric material secured to a surface of said first semiconductor device, a second semiconductor device **152** positioned over said first semiconductor device, a surface of said second semiconductor device being

secured to said nonconfluent spacer layer; and the second semiconductor device, including a back side secured to the nonconfluent spacer layer.

(69) The conductive epoxy 160 and glass spheres 162 shown in FIG. 15 provide an electrical interconnection between relocated pads 194 in the bottom die 152 and the relocated pads 184 on the top die 150 in a flip chip arrangement as well as maintaining a certain distance between die 150, 152.

20. The semiconductor device assembly of claim 19, Vindasius et al. show wherein said nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of said nonconfluent spacer layer.

21. The semiconductor device assembly of claim 20, Vindasius et al. show wherein said at least one void facilitates lateral introduction of adhesive material between said first and second semiconductor devices.

22. The semiconductor device assembly of claim 19, Vindasius et al. show wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. The semiconductor device assembly of claim 19, Vindasius et al. show wherein said nonconfluent spacer layer has a substantially uniform thickness.

24. The semiconductor device assembly of claim 19, Vindasius et al. further comprising: at least one discrete conductive element protruding above a surface of at least one of said first and second semiconductor devices and located at least partially between said first and second semiconductor devices.

25. The semiconductor device assembly of claim 24, Vindasius et al. show wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that exceeds a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

26. The semiconductor device assembly of claim 24, Vindasius et al. show wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that is about the same as or less than a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

33. The semiconductor device assembly of claim 19, Vindasius et al. show wherein said nonconfluent spacer layer comprises a pattern.

34. The semiconductor device assembly of claim 19, Nakanishi et al. show wherein said nonconfluent spacer layer comprises randomly arranged features.

35. The semiconductor device assembly of claim 19, Vindasius et al. further comprising: an adhesive material securing said nonconfluent spacer layer to at least one of said surface of said first semiconductor device and said surface of said second semiconductor device.

36. The semiconductor device assembly of claim 35, Vindasius et al. show wherein said adhesive material is located within voids in said nonconfluent spacer layer.

In claim 37, Vindasius et al. show a substrate **154** upon which one of said first semiconductor device **152** and said second semiconductor device **150** is positioned.

In claim 38, Vindasius et al. show at least one bond pad of at least one of said first semiconductor device **152** and said second semiconductor device **150** is in communication with a corresponding contact area of said substrate **154**.

In claim 39, Vindasius et al. show the substrate comprising at least one of **a circuit board**, an interposer, another semiconductor device, and leads.

40. The semiconductor device assembly of claim 19, Vindasius et al. show wherein said nonconfluent spacer layer is positioned between an active surface of said first semiconductor device and a back side of said second semiconductor device.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a nonconfluent spacer layer and a plurality of layers deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and

stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 42 to 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent # 6,437,449 B1).

42. The semiconductor device assembly of claim 19, Foster show wherein the nonconfluent spacer layer **216** comprises a plurality of layers (portions of 216), additive thickness of the plurality of layers defining substantially the same distance.

43. The semiconductor device assembly of claim 42, Foster show wherein a first layer of the plurality of layers (one portion of 216) is secured to the active surface of the first semiconductor device and a second layer of the plurality of layers is configured to be secured to the back side of the second semiconductor device.

44. The semiconductor device assembly of claim 42, Foster show wherein at least some solid regions of each of the plurality of layers (216) are at least partially superimposed relative to one another.

Therefore, it would have been obvious to one of ordinary skill in the art to use the nonconfluent spacer layer and the plurality of layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 42 to 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vindasius et al. (U.S. Patent # 6,098,278).

42. The semiconductor device assembly of claim 19, Vindasius et al. show wherein the nonconfluent spacer layer **162** comprises a plurality of layers 160,162, additive thickness of the plurality of layers defining substantially the same distance.

43. The semiconductor device assembly of claim 42, Foster show wherein a first layer of the plurality of layers (one portion of 162,160) is secured to the active surface of the first semiconductor device and a second layer of the plurality of layers is configured to be secured to the back side of the second semiconductor device.

44. The semiconductor device assembly of claim 42, Foster show wherein at least some solid regions of each of the plurality of layers (160,162) are at least partially superimposed relative to one another.

Therefore, it would have been obvious to one of ordinary skill in the art to use the nonconfluent spacer layer and the plurality of layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (U.S. Patent Application Publication # 2001/0013643) in view of Smith, Jr. et al. (U.S. Patent # 6,049,370).

Nakanishi et al. show the features of the claimed invention as detailed above, but fail to explicitly show a spacer layer comprising polymer, where as the polymer comprises a photoimageable polymer. Shimi does discloses that the jumper strips 50A, 50B, and 50C can be made of a variety of insulative materials and by a variety of techniques. For example, they can be fabricated from a resin tape or a sheet of fiberglass impregnated with an epoxy resin using conventional circuit tape or PCB fabrication techniques. Photoimageable polymer is defined to be a photoresist polymer.

Smith,Jr. et al. is cited for showing liquid crystal light valvue using internal, fixed spacers. Specifically, Smith, Jr. et al. (figures 2 to 5) specifically figure 3 discloses a ariety of materials may be used to form the spacer pads 40, including an oxide, such as silica or indium tin oxide, a metal, such as chromium, aluminum, or gold, and polymers, such as polyimides or photoresist materials for the purpose of giving spacing between electrical connecting materials.

Therefore, it would have been obvious to one of ordinary skill in the art to use Smith, Jr. et al.'s photoresist polymer spacer to modify Nakanishi et al.'s spacers for the purpose of giving spacing between electrical connecting materials.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (U.S. Patent Application Publication # 2001/0013643) in view of Blanton (U.S. Patent # 5,220,200).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers deals with an issue (i.e., the integration of multiple pieces into one

piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure. Nakanishi et al. dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers.

Blanton is cited for showing provision of substrate pillars to maintain chip standoff. Specifically, Blanton (figures 1 to 3) specifically figure 3 discloses dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers for the purpose of providing standoff means to space an integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to use the dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers as "merely a matter of obvious engineering

choice" as set forth in the above case law. However, it would have been obvious to one of ordinary skill in the art to use Blanton's series of layer to make a spacer to modify Nakanishi et al.'s spacers for the purpose of providing standoff means to space an integrated circuit.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent # 6,437,449 B1) view of Blanton (U.S. Patent # 5,220,200).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Foster's dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers.

Blanton is cited for showing provision of substrate pillars to maintain chip standoff. Specifically, Blanton (figures 1 to 3) specifically figure 3 discloses dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers for the purpose of providing standoff means to space an integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to use the dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers as "merely a matter of obvious engineering choice" as set forth in the above case law. However, it would have been obvious to one of ordinary skill in the art to use Blanton's series of layer to make a spacer to modify Foster's spacers for the purpose of providing standoff means to space an integrated circuit.

Claims 18 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vindasius et al. (U.S. Patent # 6,098,278) in view of Blanton (U.S. Patent # 5,220,200).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured

as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure. Vindasius et al. dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers.

Blanton is cited for showing provision of substrate pillars to maintain chip standoff. Specifically, Blanton (figures 1 to 3) specifically figure 3 discloses dielectric layer can be a plurality of at least partially superimposed, contiguous, adhered sublayers for the purpose of providing standoff means to space an integrated circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to use the dielectric spacer layer and a plurality of at least partially superimposed, contiguous, adhered sublayers as "merely a matter of obvious engineering choice" as set forth in the above case law. However, it would have been obvious to one of ordinary skill in the art to use Blanton's series of layer to make a spacer to modify Nakanishi et al.'s spacers for the purpose of providing standoff means to space an integrated circuit.

Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (U.S. Patent Application Publication # 2001/0013643) in view of Mueller et al. (U.S. Patent # 6,316,786 B1).

Nakanishi et al. show the features of the claimed invention as detailed above, but fail to explicitly show a spacer layer comprising (all types) at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

Mueller et al. is cited for showing an organic opto-electronic devices. Specifically, Mueller et al. (figures 1A to 3c) specifically figure 1B discloses spacers 13 and 15 comprising silicon nitride, SiN.sub.x, SiO.sub.x, SiO.sub.2, Siliconoxynitride (SiON), organic compounds such as polyimides, aluminiumoxide, aluminiumnitride, or titaniumoxide, for example for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mueller et al.'s spacer to modify Nakanishi's spacers for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent # 6,437,449 B1) in view of Mueller et al. (U.S. Patent # 6,316,786 B1).

Foster show the features of the claimed invention as detailed above, but fail to explicitly show a spacer layer comprising (all types) at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

Mueller et al. is cited for showing an organic opto-electronic devices. Specifically, Mueller et al. (figures 1A to 3c) specifically figure 1B discloses spacers 13 and 15 comprising silicon nitride, SiN.sub.x, SiO.sub.x, SiO.sub.2, Siliconoxynitride (SiON), organic compounds such as polyimides, aluminiumoxide, aluminiumnitride, or titaniumoxide, for example for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mueller et al.'s spacer to modify Foster's spacers for the purpose of providing sufficient contact between the layers and damage between the layers are avoided.

Response

Applicant's arguments filed 11/1/07 have been fully considered, but are not found to be persuasive in view of the new grounds of rejections detailed above.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,778,784-787,734,737,738,723,730,773,e25.013,e23.085,e23.052,e23.092	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04 1/23/05 5/1/05 10/18/05 7/30/07 1/13/08
Other Documentation: foreign patents and literature in 257//686,685,777,778,784-787,734,737,738,723,730,773,e25.013,e23.085,e23.052,e23.092	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04 1/23/05

	5/1/05 10/18/05 7/30/07 1/13/08
Electronic data base(s): U.S. Patents EAST	9/9/02 2/22/03 5/8/03 8/18/03 11/17/03 5/4/04 1/23/05 10/18/05 7/30/07 1/13/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
1/13/08

Alexander Williams
Primary Examiner